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Integrated Photonic Electronic platform for Quantum Technologies – INPEQUT

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ABSTRACT

The project INPEQUT addresses one of the fundamental cornerstones in the development of Quantum Technologies (QT) – implementation of a full photonic/electronic chip-scale integration enabling a shift from laboratory experiments to actual applications using portable devices. The development of (a) on-chip and scalable sources of entangled photon pairs (quantum information carriers) and (b) their efficient readout via Si detectors are the main objectives of INPEQUT, which should constitute the basis for developing compact devices operating at ambient temperatures. Both have been successfully engineered and first prototype chips have been fabricated. Final characterization of these devices is currently under progress.

Keywords: Quantum technologies; photon sources; electronic readout; full integration.

1. INTRODUCTION

INPEQUT addresses a series of challenges listed in the European QT roadmap 2016:

- it will provide a testbed for the future LOQC (linear optics quantum computing) and integration of micro-optics-based chip-scale Quantum Photonic Circuits into traditional microelectronic systems.
- Successful implementation of INPEQUT goals will provide a basis to setup a consortium formed by leading European universities, research centres and companies specialized in the field of quantum physics, informatics, photonics, laser technology and microelectronics.

The project aims at seeding the development of chip-scale integrated Quantum Photonic Integrated Circuits (Q-PIC) with close to room-temperature (RT) Single Photon Detectors, which are expected to achieve a maturity for integration into real-world devices (super-computers) within a few years from now. Thus, the project INPEQUT has an ambition to set up a smart scalable technological solution pointing to demonstrate a relevant building block for QTs, strategic for the quest for a <u>breakthrough</u> technology in Europe.

Within the project INPEQUT we have developed successfully a viable technological platform for monolithic integration of Q-PICs with Silicon Photodiodes and Single Photon Avalanche Diodes (SPADs). In particular, two designs (1st and 2nd generation), with increasing complexity, for on-chip optical coupling of photons from a Q-PIC to Silicon Detectors were designed and fabricated, while the

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optical/electrical characterization is in progress. In addition, we have successfully developed an architecture for chip-scale dispersion-engineered oxynitride (SiON)based ring resonators for the entangled photon sources. Finally, a prototype platform for the electrical control and readout of the chip and simultaneous IN/OUT coupling of optical signals has been realized (Fig.1).



Fig. 1. The prototype photonic/electronic chip wire-bonded onto a PCB board for electrical control and readout. Inset shows an optical micrograph of the on-chip project logo.

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2. STATE OF THE ART

The simulation of quantum mechanical systems using conventional computers, requires resources, which grow exponentially with the system size. Quantum Simulators [1] (OS) are devices that operate according to the laws of quantum mechanics and possess the capability to simulate a broad range of quantum phenomena that lay beyond the classical computer capabilities [see Quantum Manifesto]. QS can truly exploit the quantum advantage over classical supercomputers when reaching a high enough number of errorless qubits, in the order of 100. QS promise to deliver a new paradigm for applications in science and engineering without the daunting resource overhead required for universal quantum computation. The calculation of a given Hamiltonian spectrum is a problem with wide applications, and can be used, e.g., to study reaction rates in quantum chemistry [2] or high-T superconductivity [3].

While partial integration of the different capabilities required for QS's has been tested, a stand-alone quantum/classical processor has still to be realized. Sources of single photons and active control of optical qubits, the potential for source scalability in silicon [4] and silica integrated devices [5] as well as waveguide-coupled high-efficiency single photon detectors [6] have been demonstrated in the past years. Silicon Nitride – an alternative CMOS compatible platform for quantum photonic circuits – is emerging in the last years, though main quantum science-oriented demonstrators focus to the Infrared (1.55 μ m wavelength) Telecom C-band [7].

3. BREAKTHROUGH CHARACTER OF THE PROJECT

Single photon sources and detectors have not been integrated together on the same chip due to challenges in removing the laser light used to pump the non-linear photon source. The integration of the these required components needed for optical Quantum Simulations, compared to the state-of-the-art demonstrations [5] [8] [9] will provide a decisive improvement towards a scalable architecture. The targeted breakthrough of INPEQUT is thus the demonstration of a monolithically integrated "Quantum photonic circuit – Single-photon-resolving" scalable and compact system operating at room temperature.

At the core of the INPEQUT, a quantum photonic chip based on a low-loss (\leq 1dB/cm) SiON platform and operating at NIR wavelengths (800-850nm) will be developed. The use of the low index and low loss SiON material will enable a monolithic integration of the photonic circuits (generation and manipulation of entangled photons, Mach-Zehnder interferometers) with silicon SPADs on the same chip – a far-reaching goal that will represent a leap forward in the field of photonic quantum technologies.

To achieve this goal, we aim to merge our existing capabilities in areas of (i) integrated photonic devices, (ii) quantum optics and spectroscopy, (iii) silicon single-photon detectors and (iv) advanced electronic control and readout circuitry.

Thus, the project INPEQUT <u>represents an ambitious and</u> <u>concrete step</u> towards transformative advances in quantum science, industry, and society. In fact, a possible successful follow-up phase of INPEQUT is expected to fill up the existing gap between the largely advanced fundamental knowledge of Quantum Science and technologically uncertain industrial sector. As an example, we envision the concrete possibility to develop a compact 3D-integrated quantum simulator (QS), where a photonic quantum interference circuit will be fully integrated with scalable on-chip sources to generate quantum states of light within nonlinear SiON waveguides, terminated with single-photon detectors (Si SPADs) and electronic readout.

4. PROJECT RESULTS

A. Waveguide-to-Detector Coupling

Our project started with the development of an appropriate coupling between photonic components (integrated dielectric waveguides) and Si photodetectors (PD). This approach focuses on the optical engineering of the waveguide by means of cross-section squeezing, such that the propagating electromagnetic field leaks efficiently towards the PDs situated at the substrate level below the PIC. The first generation of devices was successfully fabricated (Fig. 2a) and tested.

A first testing of the opto-electronic response of the Si PDs was performed under normal incidence conditions revealing adequate responsivities at the NIR wavelengths (800-850nm) on the order of ~1A/W, in line with FBK's technology. In a second step, the chips were wire bonded onto PCB boards to allow simultaneous optical-electrical measurements (Fig. 1), where the light was injected into the waveguides and the evanescent photon field was successfully detected through the PDs (Fig. 2b).

Next, a second generation of devices were studied and designed for PIC-to-SPAD coupling. In this case, an optical engineering of the bottom SiO2 cladding, which isolates the PIC from the Si substrate, was sought based on our previous technological developments [10]. The fabrication of these devices is at an advanced stage currently. We expect a photon detection efficiency (PDE) of 40-50% under single-photon operation, which may become >80% upon further optimization.

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Fig. 2. The PIC-to-PD coupling: (a) Optical micrograph of the coupled waveguide/detector chip. (b) Light extraction from the waveguide by the underlaying PD. The strong attenuation of the light signal within the PD region is clearly visible. **The Entangled Photon Source:** (c) The engineered GVD of the entangled photon source. The Z-GVD point is indicated with red arrow. (d) The optical image of a fabricated ring resonator device (narrow pink ring) and the metallic microheaters (orange) for thermo-optical tuning.

The fabricated chips were sent recently to the Partner group at ETH-Z were additional experiments will be performed.

B. The Entangled Photon Source

In parallel, we have developed a viable platform for the on-chip generation of entangled photons via non-linear spontaneous Four Wave Mixing (sFWM) in ring resonator devices with appropriately engineered Group Velocity Dispersion (GVD). In particular, we have performed intensive numerical simulations in order to find the best geometry for single optical mode SiON ring resonators which show a zero-GVD point within the spectral region of interest between 800-850nm (Fig. 2c). Coupling of the ring resonators to input and output waveguides was carefully studied, and curved pulleytype couplers were designed accordingly.

The characteristics of real devices often deviate from the simulated and designed ones due to the imperfections of the fabrication process. Spectral features of small-sized ring resonators, in particular, can appear up to several nm's away from the designed wavelengths. Moreover, the spectra of nominally identical devices, spatially situated 100 μ m apart on the same chip, may differ from each other. This issue may become the bottleneck on the way of developing scalable architectures of entangled photon sources, where the demand is to realize "identical" devices, all aligned spectrally to the same pump laser wavelength.

For this, we have designed also metallic micro-heaters to be integrated directly on the chip during the fabrication process (Fig.2d). The basic principle of operation of micro-heaters is to produce local Joule heating when electrical current flows through the resistor. The absorbed heat changes the refractive index of the optical component's material and thus allows for small-range spectral tuning of the ring resonators.

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Several wafers with such devices were fabricated, and first passive optical characterization was performed. These first experiments showed that the propagation losses are low (good optical quality) and in line with the expected values (Fig. 3).

In a next step, we plan to perform nonlinear sFWM experiments in order to generate entangled photon pairs directly on-chip. For this, the fabricated chips are being prepared to be sent to the Partner group at ETH-Z were nonlinear experiments of sFWM will be conducted during the next months.

C. Scientific output

A scientific-style paper, describing the results of Waveguide-to-Detector Coupling of the first-generation devices, is currently under preparation and is intended for publishing in a high impact international journal in the optics/photonics domain. Parts of the electrical characterization and control of chips components have been reported in a conference paper [11].



Fig. 3. Example image of the passive optical characterization of propagation losses in the PICs. The light is butt-coupled to the chip via an optical fiber, and the amount of light, transmitted through spiral waveguide structures, is collected at the output.

In addition, two detailed internal reports (not available for public) have been produced for research lines above described in subsections A and B, that may be available for ATTRACT Consortium upon request.

5. FUTURE PROJECT VISION

The project EPIQUS

An EU Commission H2020 FET Open proposal (EPIQUS), composed of a consortium of 8 partners and coordinated by the PI of INPEQUT, has been recently selected for funding to build an Integrated Photonic Quantum Simulator. This 3.5Y project will be starting on 1st of October 2020 and will implement few basic concepts developed within the ATTRACT INPEQUT project. The overall goal of the project EPIOUS will be the development of a 3D-integrated quantum simulator hardware, where (1) a photonic quantum interference circuit, hosting (1a) scalable entangled photon sources, (1b) the state preparation stage and (1c) the 16 qubit reconfigurable quantum interference circuit, will be monolithically integrated on the same Si chip with (2) scalable arrays of SPADs operating at ~850nm and at RT. Our consortium will build an integrated system, in which on the "software level" a quantum algorithm will sustain the quantum simulation results from the hardware. A custom Analog chip will control the QS module by managing the pump laser, phase shifters and the SPADs in order to control actively the quantum optical circuit. Finally, the output data will be handled by the digital chip to feed the software algorithm. EPIQUS will envision scalability up to 50 qubits using the proposed breakthrough technology.

Envisioning ATTRACT Phase 2

In view of the Phase 2, developments from INPEQUT can be used for setting up another H2020 FET-type proposal. In particular, the developed technology for onchip PIC-to-SPAD coupling appears to be a universal key enabling technology for several type of research directions – from Brillouin and Raman spectroscopy to Optical Gyroscope applications. In all of these cases, a possible miniaturization via chip-scale integration should necessarily run through highly efficient coupling of micro/nano-photonic functionalities (optical domain) and an electronic control and readout (photon detection).

At the current stage of development of above-mentioned research directions, these activities have a larger probability in pointing to real applications and market. Currently, we are envisioning possible collaborations with players from research, SME's, and industry in some of the mentioned directions.

5.1. Technology Scaling

Within INPEQUT we have successfully merged the separate technologies for the photonic circuitry (TRL3/4) and the SPAD devices (TRL7/8). Thus, while the PIC-to-Detector coupling was at a TRL 1/2 level at the moment of writing the INPEQUT proposal for Phase 1, now it has achieved a **TRL 4** via testing and validating our technology in the lab.

The FET Open project EPIQUS is pointing to bring the fully integrated photonic-electronic Quantum Simulator to a TRL6 level by demonstrating a free-running QS hardware-software system.

5.2. Project Synergies and Outreach

The EPIQUS consortium includes 5 universities, two research institutions and an industrial partner. In case of an ATTRACT Phase 2 proposal, aiming to develop e.g. a chip-integrated Brillouin spectrometer, we will need partners from university groups for the fundamental science and experimental side, company(ies) with expertise in Diagnostic applications as well as SME's to allow for packaging and system integration.

A detailed dissemination plan will be elaborated (webpage, open access scientific journals and data repositories).

5.3. Technology application and demonstration cases

The technology demonstration cases that will be implemented in ATTRACT Phase 2 bring benefit to the areas *Health, demographic change and wellbeing,* while the FET EPIQUS project will point to the case of *Secure societies - protecting freedom and security of Europe and its citizens.* Both cases have the potential to bring benefit to the Research Infrastructure communities in Europe. In particular, seven partners of EPIQUS are EU-situated. Similar approach will be applied for a possible Phase 2 project provided that all necessary expertise is available in EU.

5.4. Technology commercialization

We will contact technology stakeholders and companies in order to exploit developments and results, and, in general, to accelerate awareness that a technological breakthrough is necessary for the future of Quantum Technologies in case of EPIQUS.

The presence of end-user Companies and industrial partners within the consortium for a possible ATTRACT Phase 2 project will be essential for planning a rapid commercialization.

5.5. Envisioned risks

Possible risks, related to the technological developments, will be continuously monitored, and their Mitigation plans elaborated and followed throughout the duration of the project.

Examples of risks can be related to (i) non-uniformities of photonic components on the wafer-scale, (ii) electronic interconnection capacitances or (iii) dark counts of SPADs. These may be mitigated by relaxing correspondingly dimensions of photonic devices on cost of larger footprint, considering advanced flip-chip bonding techniques, and employing shorter gate pulses, diminishing excess bias voltages, or using smaller area detectors.

5.6. Liaison with Student Teams and Socio-Economic Study

In a possible Phase 2 project we will nominate an experienced person who will provide with MSc. level explanation materials of our technology. In addition, the project will organise dedicated Workshops to disseminate our results as well as Schools to train future students. The workshops will be open to academic and industrial groups outside the consortium, with selected key leaders invited to participate.

We will address the Public through articles in popular science magazines, by giving interviews, and participation in TV/radio shows or Open days and science festival demonstrations.

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